IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application Inventors: Charles A. Miller Appli. No.: 10/693,133 Confirm. No.: 1801 Filed: October 23, 2003 Title: ISOLATION BUFFERS WITH CONTROLLED EQUAL TIME DELAYS	PATENT APPLICATION Art Unit: 2829 Examiner: Kobert, Russell Marc **Customer No. 23910**

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Susan Bouchard (Signature)

Signature Date: June 15, 2006

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
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Sir:

The Remarks provided in this Pre-Appeal Brief Request for Review respond to the Advisory Action Before the Filing of An Appeal Brief, mailed on March 31, 2006 (the "Advisory Action"), and address the rejections set forth by the examiner in the Final Office Action mailed on December 15, 2005 (the "Final Office Action").

The present invention relates to, *inter alia*, a system for testing integrated circuits on a wafer, including a single test signal channel of the wafer test sytem connected to multiple test probes through isolation buffers to prevent signal degradation. Claims 1-13 and 24 are pending in the Application. The Final Office Action and the Advisory Action note that certain claims stand rejected, while the others were deemed allowable or objectionable. Only the rejected claims are appealable, and are addressed in this Pre-Appeal Brief Request for Review (the "Pre-Appeal Brief"); they are claims 1 and 24.

Regarding claim 1, the Final Office Action maintained the previous rejections under 35 U.S.C. § 102 from the previous Non-Final Office Action, mailed on March 7, 2005. Specifically, claim 1 stands rejected under § 102(e) as anticipated by U.S. Patent No. 6,622,103 to Miller. In the Final Office Action, claim 24 stands rejected under § 103(a) as being unpatentable over Miller in view of U.S. Patent No. 5,070,297 to Kwon et al. (hereinafter "Kwon"). Only claim 1 is addressed below, as claim 24 is believed allowable based on its dependency on claim 1.

Section 102(e): Claim 1 is not Anticipated by Miller

Claim 1 as amended claims:

> An apparatus comprising:
>
> ¶ a *variable delay isolation buffer* having a signal input, a signal output, and a variable delay control input *for selectively varying a delay caused by the variable delay isolation buffer in a signal traveling from the signal input to the signal output*; and
>
> ¶ a *delay control circuit* having an output providing the variable delay control input of the variable delay isolation buffer, the delay control circuit *setting a delay control voltage potential at its output to control delay through the variable delay isolation buffer* to substantially match delay through a time delay reference.

Applicant has argued that claim 1 as amended is not anticipated by Miller because Miller does not teach or disclose "a *variable delay isolation buffer*" having a "control input *for* selectively varying a delay caused by the variable delay isolation buffer in a signal traveling from the signal input to the signal output."

In response, the examiner argued that Miller discloses at col. 7, line 67 that the "Z signal delay" is calibrated, requiring it to be selectively varied. Further, the examiner argued that Miller discloses in col. 6, lines 34-37, the use of a computer timing circuit 46 for timing of the Z, DRIVE, and COMPARE signals, rendering claim 1 anticipated. Furthering these two arguments, the examiner states that Miller anticipates claim 1 of the present invention because the intended use required by claim 1 must present a structural

difference, or if the prior art cited is capable of performing the intended use, it meets the claim limitation. Final Office Action at 3. In the Advisory Action, the examiner argued that a "whereby clause in a method claim is not given weight when it simply expresses the intended result of a process step positively recited," quoting Minton v. Nat'l Ass'n of Securities Dealers, Inc., 336 F.3d 1373, 1381 (Fed. Cir. 2003). Advisory Action Continuation of 11. Applicant respectfully disagrees that claim 1 is anticipated, for the following reasons.

First, Applicant maintains that delaying the Z signal in Miller using *computer timing circuit 46 does not delay the buffer output* as in claim 1, it *only delays disabling of the tri-state buffer 40.* In Miller, the tri-state buffer is tri-stated by the Z signal, so the tri-state buffer 40 either enables an output signal with the Z signal in one state, or disables the output signal with the Z signal in another state. A tri-state buffer typically has an output gate that enables or disables the output signal, and does not vary any delay provided into and through the buffer. Use of the computer timing circuit for timing of the Z signal to the tri-state buffer does not delay the buffer output but instead delays when the buffer output is disabled.

In contrast, Applicant's claim 1 and specification call for a *variable delay* isolation buffer, configured like the buffer 51 of Fig. 12, and not a tri-state buffer. As shown in Fig. 12, the power supply voltage V_H and V_L are changed to control the delay of signals through the buffer 51. As shown in Fig. 10, V_H and V_L have operating ranges providing the "delay control voltage potential" set by the delay control circuit "as its output to control the delay through the variable delay isolation buffer" of claim 1. The buffer circuitry of Fig. 12 can be used in the variable delay isolation buffer 110 of Fig. 11, or buffers 50_1 and 50_2 of Fig. 8. Thus, a true signal delay is provided by Applicant's variable delay isolation buffer, in contrast with the Z signal in Miller that only enables or disables the buffer output, to form the tri-state buffer 40.

Second, the *calibration of the "Z signal delay"* of Miller that may require it to be selectively varied also *only requires it to delay disabling of the buffer.* As discussed above, the delay control circuit of the present invention, on the other hand, changes the power supply voltage V_H and V_L to control the delay through the buffer 51. Again, delaying the Z signal in Miller using computer timing circuit 46 does not delay the buffer output as in claim 1, it only delays disabling of the tri-state buffer 40.

Third, Applicant maintains the tri-stating buffer 40 receiving the *Z signal* of Miller is *not capable of performing the intended use of the variable delay isolation buffer* of claim 1. (see Miller, col. 6, line 28). The applicant believes the intended use in claim 1 the examiner refers to is "for selectively varying a delay caused by the variable delay isolation buffer in a signal traveling from the signal input to the signal output." As discussed above, a tri-state buffer, like that tri-state buffer of Miller, typically has an output gate that enables or disables the output signal, and does not vary any delay provided through the buffer.

Fourth, Applicant disagrees that the intended use required by claim 1 does not present a structural difference, as the *variable delay isolation buffer itself presents a different structure than the tri-state buffer.* The term "tri-state buffer" stands on its own as a type of buffer. Functional language in its name "tri-state" identifies the structure of the buffer. Similarly, other patents, such as U.S. Patent Nos. 5,467,041 and 5,687,177, show the term "variable delay buffer" has a structure known to a person of ordinary skill. Thus, the term "variable delay isolation buffer" in claim 1 stands on its own as a type of buffer known to a person of ordinary skill, as the term "variable delay" describes the buffer.

Finally, the Applicant disagrees that MPEP 2111.04 is applicable to claim 1, or that a "whereby clause in a method claim is not given weight when it simply expresses the intended result of a process step positively recited," quoting Minton, applies to claim 1. First, claim 1 does not include any of the language "adapted to," "adapted for,"

"wherein," or "whereby" addressed by MPEP 2111.04. As indicated above, the name "variable delay isolation buffer" presents sufficient structural difference without further result language. Further, Minton is not believed applicable because claim 1 is an apparatus claim, and not a method claim, as referenced by Minton. Further, Minton addresses a descriptive "whereby" clause, as opposed to the language of claim 1.

For the above reasons, Miller does not teach or suggest the "variable delay isolation buffer" as claimed in claim 1, and as supported by Applicant's specification. For these reasons, claim 1 is thus believed allowable as not anticipated under 35 U.S.C. § 102 by Miller.

Conclusion

In light of the above remarks, claims 1-13 and 24 are now all believed to be in condition for allowance. Accordingly, reconsideration and allowance of these claims is respectfully requested.

A Notice of Appeal is included herewith.

Respectfully submitted,

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